# A CMOS 802.11b Wireless LAN Transceiver

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*Abstracts* — **This paper describes a 2.4 GHz 0.25 μm CMOS RF transceiver chip that has the potential to be used in place of a SiGe transceiver chip used in an 802.11b radio. The 802.11b radio with the CMOS transceiver was tested along with the radio with SiGe transceiver. CMOS radio transmits RMS power of 13.1 dBm at antenna output while the SiGe radio has 13.2 dBm output power. CMOS radio receiver has sensitivity of -81 dBm at 11Mbps while the SiGe receiver has sensitivity of -84 dBm. Overall, the radio with CMOS transceiver consumes 5% more current than the one with SiGe chip.**

## I. Introduction

IEEE 802.11b based Wireless Local Area Network (WLAN) systems have enjoyed robust growth over the past few years [1]. With this growth, there has been accompanying pressure on price. To address this, a 2.4-GHz 0.25-μm CMOS RF transceiver chip is developed. This RF CMOS transceiver can be used to implement a PRISM II.5 802.11b radio which has comparable power consumption as radios using a transceiver fabricated in a SiGe BiCMOS process.

## II. System Overview

The radio shown in Figure 1 employs a traditional superheterodyne architecture. On the receiver side, the antenna is routed to a ceramic band pass filter (BPF) which attenuates out of band signals as well as the 1.7 GHz image signal. The received signal then goes to the RF transceiver chip which converts the signal at an RF frequency between 2.400 and 2.484 GHz (ISM band) to an IF frequency of 374 MHz. An RF synthesizer is included in the IC with an off-chip VCO. On the transmitter side, the same RF transceiver converts the signal at 374 MHz to an RF frequency in the ISM band. A power amplifier (PA) then boosts the signal to around 15 dBm. A differential 374 MHz channel selection SAW filter follows the RF transceiver. A separate IF chip converts the received signal after the SAW to baseband (receive mode) or modulates the baseband transmit signal to IF (transmit mode). The baseband processor (BBP) implements the IEEE 802.11 CCK modulation. The MAC serves as a digital interface between the 11 Mbps data and computer/controller.

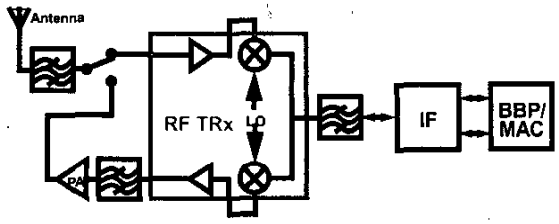


Fig. 1, An 802.11b WLAN Radio

Contrary to the conventional wisdom, a superheterodyne WLAN transceiver can consume less power than a direct conversion transceiver. The main reason is that most direct conversion transceiver chips use differential design techniques to prevent LO leakage through the substrate, bond wires and package. The superheterodyne transceiver circuits, on the other hand, are mostly single-ended. Another reason is that, since the channel selection is performed by a SAW filter, the dynamic range of the subsequent IF and baseband circuits can be relaxed. On top of that, the extra circuitry associated with DC offset cancellation in direct conversion transceiver is avoided, resulting in both power and die area reduction. The image problem associated with a superheterodyne receiver can be tackled by careful frequency planning. If the image is located in a quiet band and is far away from carrier frequency, the front-end band pass filter and the tuned response of LNA/Mixer render more than 50 dB of image rejection, obviating the need of an external image rejection filter. This means use of the superheterodyne architecture requires one external filter versus one or two external baluns typically needed for direct conversion radios. Because of these, fundamentally, the differences in PC board area and external component cost for the two radio architectures should be small.

## III. Transceiver Circuits

Figure 2 shows the components of the RF transceiver chip. The receiver chain features a low noise amplifier (LNA), followed by a down conversion mixer [2]. The



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transmit chain consists of an up conversion mixer and a transmit amplifier (TXA). The remaining circuitry comprises an RF Phase Locked Loop (PLL) frequency synthesizer and on-chip LO buffers: the LO signal is generated by an off-chip VCO and comes into the RF transceiver chip single endedly. It is converted to differential using an on-chip converter. This differential signal is then buffered through three source followers and amplified to drive the mixer switching cores in the Rx and Tx mixers as well as the clock of the prescaler.

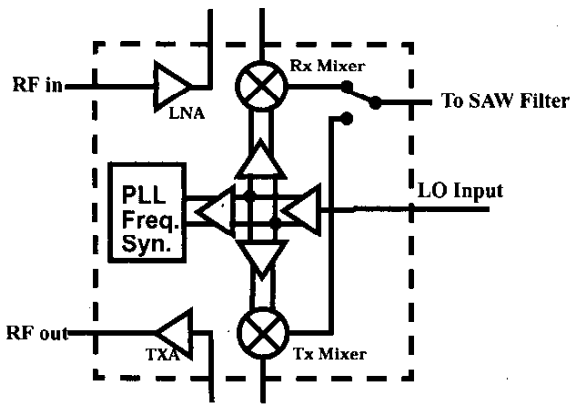


Fig. 2, RF Transceiver

The output of LNA is not connected to the Rx mixer input directly on-chip. The RF output signal from LNA goes off-chip first and then back on-chip to the Rx mixer input. This provides flexibility of system design since an off-chip Image Rejection Filter (IRF) can be placed here to boost the image rejection if necessary. As mentioned, good frequency planning can make the IRF not necessary. The output of LNA and input of Rx mixer are connected directly in an off-chip 50 Ω environment to form the receiver chain. Similar situation occurs at the transmitter side where the optional band pass filter (BPF) after the Tx mixer is not present. The output of the Tx mixer and the input of Tx amplifier are connected directly off-chip to form the transmitter chain.

The CMOS transceiver IC is fabricated in a 0.25 μm foundry logic CMOS process. For low cost, MIM capacitor and high resistance resistor options are not used. Instead, capacitors are formed using the free MOS structure [3], while resistors are formed using the gate polysilicon layer. Figure 3 shows the micro-photograph of the CMOS chip. The CMOS IC has a die area of 2.5 mm x 2.5 mm which is slightly smaller than that of the SiGe transceiver. It is also housed in the same 44 pin Micro Lead Frame (MLF) package so its pinout can be compatible.

Most of the RF circuits in CMOS transceiver are implemented using the same topology and similar schematic as their SiGe counterparts. LNA's are single stage cascode amplifiers with inductive degeneration while the Rx mixers are Gilbert type double balanced active mixers [2]. Figure 4 shows the CMOS Tx mixer schematic. Figure 5 shows the schematic of CMOS TXA. CMOS TXA assumes a single stage, common source cascode configuration. Usually the noise figure is not a huge concern in transmitter design so the input of the TXA is matched with an on-chip inductor. The frequency synthesizer is an integer N charge pump PLL with a dual-modulus divide-by 32/33 prescaler [4]. The loop filter is off-chip.

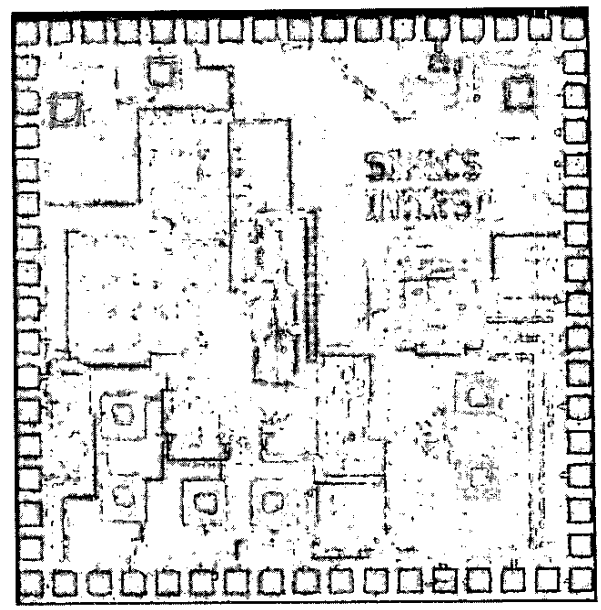

Fig. 3, Micro-photograph of CMOS RF transceiver

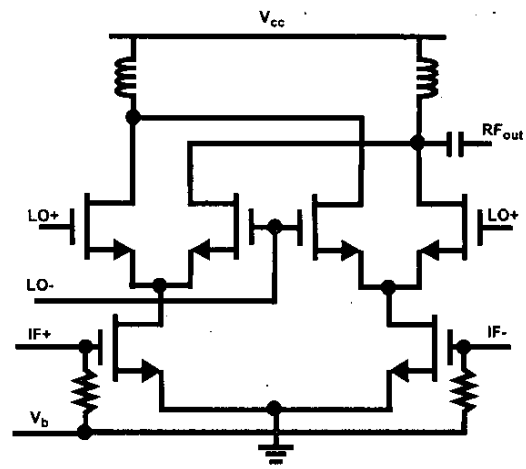


Fig. 4, CMOS Tx mixer schematic

Table 1 compares the performance of the receiver and the transmitter of both CMOS and SiGe RF chips. CMOS receiver has 6 dB lower gain and 1.5 dB worse noise figure. CMOS transmitter has 7 dB lower gain. The $IIP_3$ and $IP_{1dB}$ of the two transceivers are close. The loop bandwidth of the

PLL frequency synthesizer is set to be 1 kHz. Phase noises of CMOS and SiGe PLL synthesizer are -81 dBc/Hz and -83 dBc/Hz at 10 kHz offset, respectively. The total current consumption of CMOS transceiver is 10 mA more (in the Rx mode) and 15 mA more (in the Tx mode) than its SiGe counterpart. Though the overall performance of the CMOS transceiver is worse than the SiGe one, its impact on WLAN radio can be tolerated due to the robustness of the superheterodyne PRISM II.5 radio. This is demonstrated in the measurement results of the WLAN radio in section IV. The missed gain of both receiver and transmitter chain are compensated by the IF AGC. The worse NF of CMOS receiver lowers the sensitivity by 3 dB. It is expected that further optimization and use of a more advanced CMOS technology (for example 0.18 μm CMOS) will narrow the differences between two chips and bring CMOS transceiver performance on par with the SiGe one.

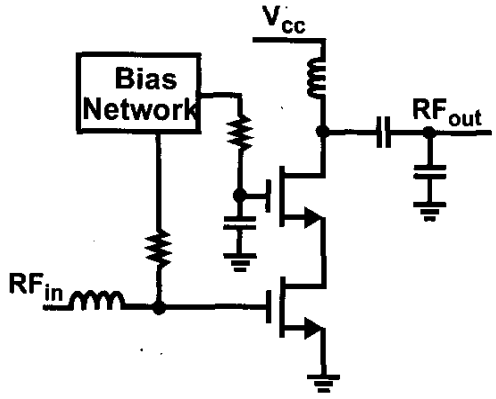


Fig. 5, CMOS Tx amplifier schematic

**Table 1: CMOS and SiGe Transceiver Comparison**

| | CMOS Transceiver | SiGe Transceiver |
|---|---|---|
| Rx Power Gain | 18.7 dB | 25 dB |
| Rx SSB NF | 5.1 dB | 3.7 dB |
| Rx Input $IP_3$ | -12.5 dBm | -12 dBm |
| Rx Input $P_{1dB}$ | -22 dBm | -23 dBm |
| Rx Current | 42 mA | 32 mA |
| Tx Power Gain | 17.5 dB | 25 dB |
| Tx Output $IP_3$ | 12 dBm | 14 dBm |
| Tx Output P1dB | 1.5 dBm | 4 dBm |
| Tx Current | 56 mA | 41 mA |
| Synthesizer Phase Noise (10 kHz) | -81 dBc/Hz | -83 dBc/Hz |

## IV. WLAN Radio Measurement

In order for the low cost CMOS transceiver to be used in place of its SiGe BiCMOS counterpart, the WLAN radio with CMOS chip has to meet the IEEE 802.11b standard and must perform close to the radio with the SiGe chip. The CMOS test chip is incorporated into a PRISM II.5 WLAN radio. The CMOS radio is measured and compared to the SiGe radio. Figure 6 demonstrates the measured transmitter

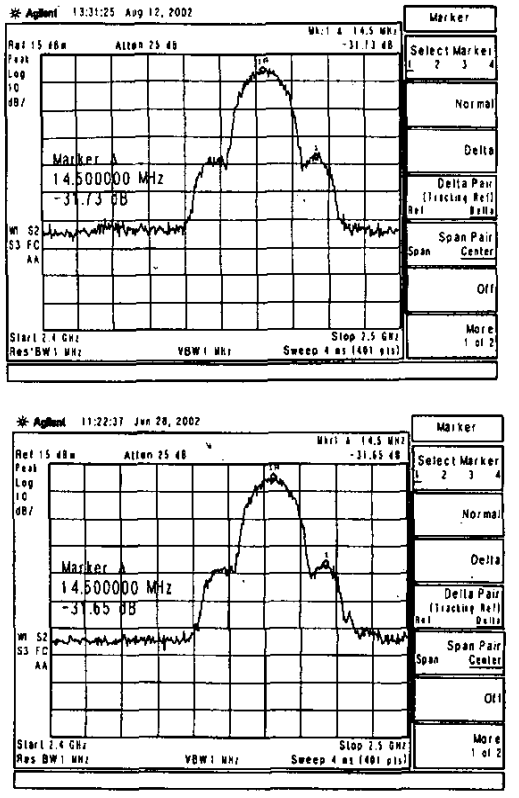


Fig. 6, Measured Transmitter Output Spectrum: Top, CMOS radio; bottom, SiGe radio.

spectra of both CMOS and SiGe radios at 11 Mbps and maximum antenna output power of 13 dBm. The first sidelobes of two transmitter are close to 31.7 dB below the main peak for both radios, meeting the 30 dB requirement of the standard. Figure 7 shows the transmitter eye patterns at the same output power level. The transmitter chain in the CMOS IC performs as well as that in the SiGe chip. Figure 8 compares the measured receiver sensitivity of the two WLAN radios at 11 Mbps data rate. The CMOS and SiGe radios have Rx sensitivity of -81 dBm and -84 dBm respectively.

Table 2 summarizes the performance of the CMOS and SiGe radios. The performance of the two radios is close. When the power consumption of the entire radio is considered, CMOS radio consumes less than 5% more current than that for the SiGe radio. The -81 dBm CMOS receiver sensi-

tivity is still 5 dB better than what's required by IEEE 802.11b standard.

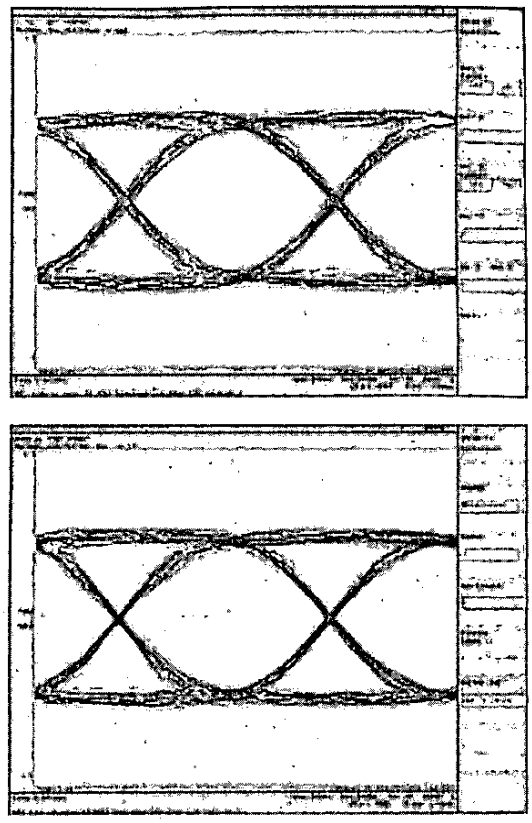

Fig. 7, Measured Transmitter Eye Pattern:
Top, CMOS radio; bottom, SiGe radio.

**Table 2: CMOS and SiGe 802.11b Radio Comparison**

| | CMOS Radio | SiGe Radio |
|---|---|---|
| Rx Sensitivity (11 Mbps, 8% PER) | -81 dBm | -84 dBm |
| Rx Image Rejection | 61 dB | 53 dB |
| Rx Adjacent Channel Rejection | 48 dBc | 50 dBc |
| Current of radio in 11Mbps Rx | 260 mA | 250 mA |
| Tx Output Power | 13.1 dBm | 13.2 dBm |
| Tx Output ACPR (1st sidelobes) | -31.7 dBc | -31.7 dBc |
| Tx Output EVM | -25.5 dB | -25.5 dB |
| Current of radio in 11Mbps Tx | 300 mA | 285 mA |

## V. Conclusion

A CMOS RF transceiver for 802.11b WLAN application is designed in a 0.25-μm CMOS technology. The CMOS transceiver is incorporated in a WLAN system and its radio performance is evaluated. The results suggest it should be possible to replace the SiGe transceiver with low cost CMOS transceivers.

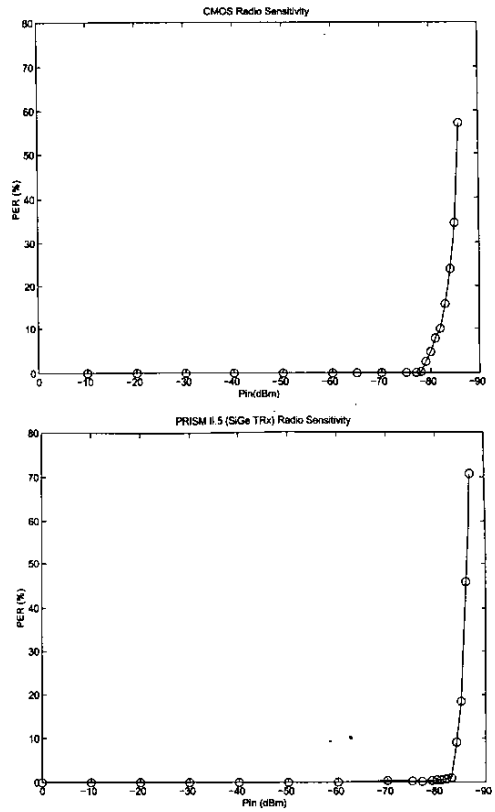


Fig. 8, Measured receiver sensitivity at 11 Mbps:
Top, CMOS radio; bottom, SiGe radio.

## References

[1] Jim Paviol, Carl Andren, and John Fakatselis, "Wireless Local Area Networks," in Microwave and RF Handbook, CRC Press, 2001.

[2] X. Li, T. Brogan, M. Esposito, B. Myers, and K. K. O, "A Comparison of CMOS and SiGe LNA's and Mixers for Wireless LAN Application," *IEEE Custom Integrated Circuits Conference*, pp. 531-534, San Diego, May 2001.

[3] C.-M. Hung, Y.-C. Ho, I-C. Wu, and K. K. O, "High-Q Capacitors Implemented in a CMOS Process for Low Power Wireless Applications", *IEEE Trans. Microwave Theory and Techniques*, Vol. 46, No. 5, pp. 505-511, May 1998.

[4] C.-M. Hung, K. K. O, "A Fully Integrated 1.5-V 5.5-GHz CMOS Phase-locked loop", *IEEE J. of Solid-State Circuits*, vol. 37, no. 4, pp 521-525, April 2002.